High Accuracy Self-Configurable DLL by Frequency Range

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Abstract — An architecture of Self-configurable Delay-Locked Loop (SCDLL) by frequency range presented in this paper. The proposed architecture produces different phases of clock signal for the different frequencies in the output of DLL over PVT, which is needed to avoid clock skew and setup/hold time margins violations between the different synchronized blocks inputs. The presented architecture is self-configurable depended on input clock signal frequencies and operates by the negative feedback system. DLL is widely used in such circuits where is the actual issue to get clock signals with different phases. For example in special input/output circuits of several standards such as Universal Serial Bus (USB), Double Data Rate (DDR) and etc.

Keywords - DLL; Voltage Controled Delay Line (VCDL); Charge Pump (CP);Frequancy To Voltage Convertor (FVC); PVT

I. INTRODUCTION

In high speed systems and interfaces, a DLL is a digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a VCDL.

The main component of a DLL (Fig. 1) is a delay chain composed of many delay gates connected front-to-back. The input of the chain (and thus of the DLL) is connected to the clock that is to be negatively delayed. A multiplexer is connected to each stage of the delay chain; the selector of this multiplexer is automatically updated by a control circuit to produce the negative delay effect. The output of the DLL is the resulting, negatively delayed clock signal.

Ordinary DLL has the structure presented in the (Fig. 1). First stage is Phase-Frequency Detector (PFD), which compares output 0^0 phase shift clock signal with 360^0 one and produces in its output signals with pulse width appropriate phase difference.

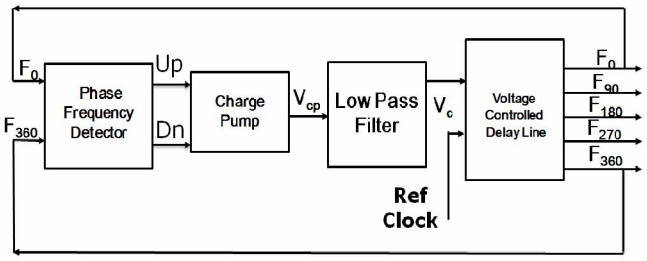

Figure 1. Main structure of DLL

Next stage is CP, which charging or discharging low-pass filter (LPF), thus generating control voltage for VCDL. Delay line produces different phases towards reference clock depended of the control voltage of CP output.

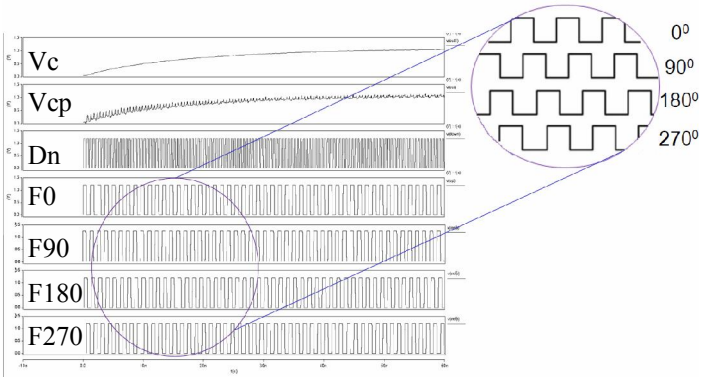

Figure 2. DLL output signals with different phases

$$(1)\ Ph\_W1 = Per / 360^0\ (ps)$$

where Per is period of signal and Ph_W1 is the 1^0 phases shift. Equation (1) shows 1^0 phase shift in picoseconds.

$$(2)\ MIN\_Ph = Per / N\ (ps)$$

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For minimum phase shift (MIN_Ph) calculation used equation (2). Where N is numbers of voltage controlled delay line cascades.

II. SELF-CONFIGURABLE DELAY-LOCKED LOOP CIRCUIT ARCHITECTURE

The structure of proposed of Self-configurable Delay-Locked Loop (SCDLL) is presented in Fig. 3.

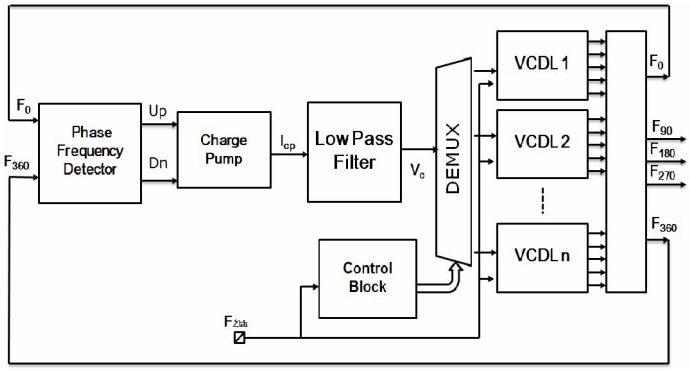

Figure 3. Proposed architecture of SCDLL

As Delay Lines can operate in some limited frequency range, so suggested circuit has different VCDLs for appropriate reference input frequencies. The selection of the VCDLs depended on the input frequencies is being implemented by control block (Fig 4), which contains 2 cascades.

First one is frequency to voltage convertor which produces analog voltages in respect of the input frequencies. Second cascade is flash analog to digital convertor (ADC) which converts gotten analog voltages to the digital codes. These codes serve as a control signals for demultiplexer (DEMUX). Depended on input digital codes DEMUX switches on a VCDL corresponding to reference frequency.

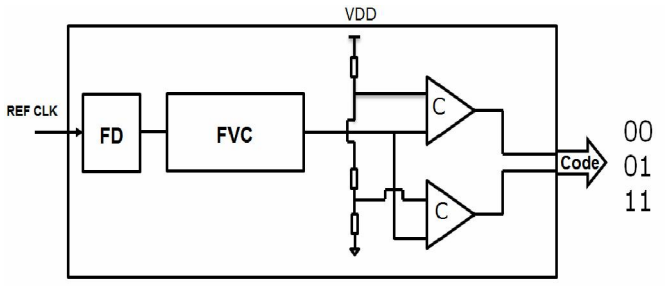

Figure 4. Control Block Structure

Designed SCDLL is operating in the frequency range between 500MHz-3GHz and taking in account the fact that FVC performs in low frequencies 40MHz-400MHz, the input stage of control block is frequency divider, which decreases reference frequency until FVC is starting to operate.

III. OPERATION PRINCIPLE AND SELF-CONFIGUREATION

Fig.5 shows low frequency FVC structure. Divided input frequency is applied to the S2 and S3 switches. During t1 time , when input signal is in login “0”, S2 switch is on and constant current charges C1 capacitance. During t2 and t3 time S2 is off, current flows to the ground through S3. When F1 signal is “1” (during t2 time), F2 is “0”, so charge distributes between C1 and C2. When F2 is “1” (during t3), F1 is “0”, so C2 isolated from the rest of the circuit and holds its charge safely during the second half of period (t1). In the same C1 capacitor discharges. After a few iterations output of C2 settles corresponding to the input reference frequency (4).

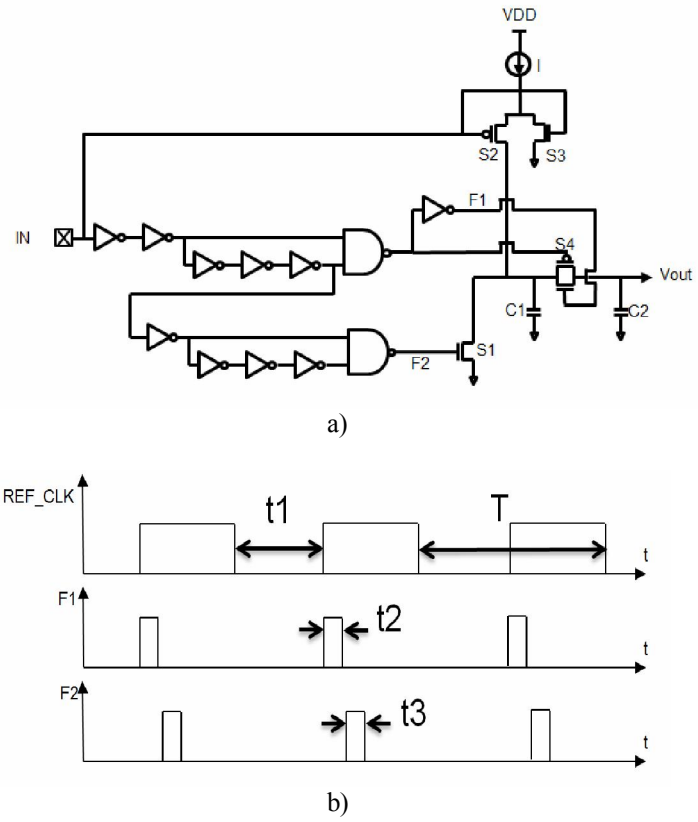

Figure 5. (a) Frequency to voltage convertor, (b) Timing diagrams of FVC

$$(3)\ V_{out} = I*t1/C$$

$$(4)\ V_{out} = (I/C)*(T/2) = (I/C)*(1/2*f)$$

For Vout voltage calculation used (3) and (4) equations, where *f* is input signal frequency.

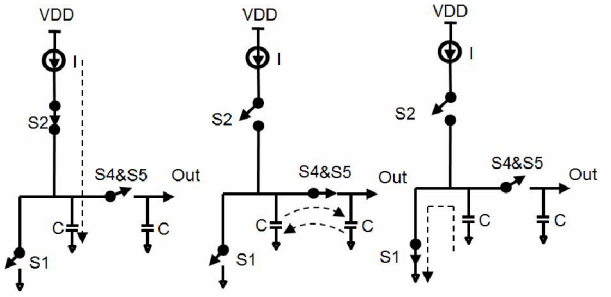

Figure 6. Operation of FVC

FVC work in 3 main operetion modes (Fig. 6). First one when initial capasitor charging during S2 switch on condition, and all others are off. Next mode begin when S4,S5 switches are on and charge distributes between 2 capacitors. And the third mode happened when initial capacitor is discharging by S1 on switch.

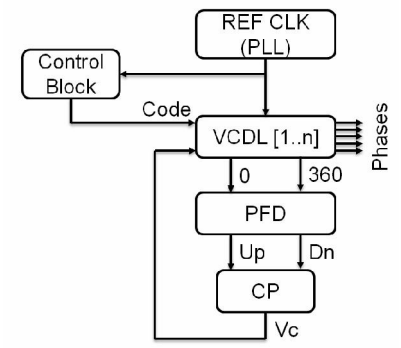

Figure 7. Block diagram of self-configurable method

As shown in Fig. 7, the SCDLL system consist from 2 loops. Frist one is standart PFD – CP – VCDL loop and when its lock in the outputs of VCDL generating different phases of reference clock. Seconde loop is VCDL – Control Block, which provide self-configuration selection correct VCDL depends on input reference signal frequancy.

IV. Simulation Results

Simulations have been performed using circuit level simulator Hspice[4] for 20 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to estimate min and max frequencies (min_freq, max_freq) and the system lock time.

Fig. 8 shows SCDLL locking results for TT(55°) typical corner. It is seen that VCDL's outputs is going to be locked after 500ns.

The next important parameter is Locking time (LT), which shows the time when SCDLL is locked. Table 1 shows results for 3 main corners.

TABLE I. Simulation results of the three main corners

Corner	PWE		Locking time
	min_freq	max_freq	
Unit	MHz	MHz	ns
TT(55)	100	2700	500
FF(-40)	100	3100	480
SS(125)	100	2500	640

Figure 8. SCDLL simulation results for TT (a), FF (b) and SS (c) corners

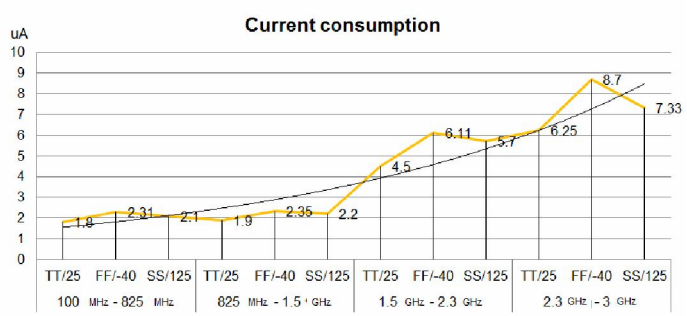

Figure 9. SCDLL current consumption for different frequency ranges

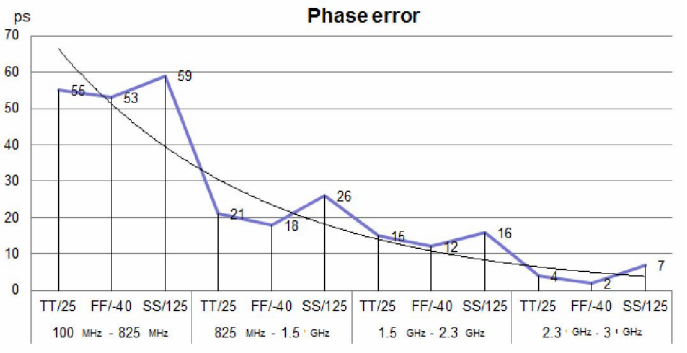

Figure 10. SCDLL phase error for different frequency ranges

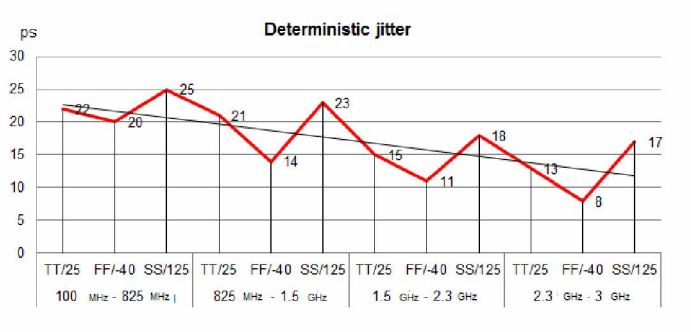

Figure 11. SCDLL DJ (deterministic jitter) for different frequency ranges

V. CONCLUSIONS

Proposed SCDLL architecture provides wide working frequency range between 100Mhz-3,1GHz. It is self-configurable circuit depended on input reference frequency. As USB3 and PCI2 protocols have 5Gb/s data rate, i.e. perform with 2.5 GHz, Designed SCDLL can be used as a clock deskewer for these standards.

Ordinary DLL has bigger area than suggested SCDLL architecture, because in standard DLLs used each Delay Line has wider frequency range than proposed one. So using control block with much more less area, this design gains in physical space and frequency range. Over PVT max frequency varies 15-24 %.

ACKNOWLEDGMENTS

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